ABSTRACT

A transistor structure is provided for ESD protection in an integrated circuit device. A semiconductor substrate has source and drain diffusion regions and respective source and drain wells under the source and drain diffusion regions. A shallow trench isolation formed over the semiconductor substrate and into the semiconductor substrate separates the source and drain diffusion regions and a portion of the source and drain wells. Source and drain contact structures respectively formed on the shallow trench isolation over the source and drain diffusion regions and extend through the shallow trench isolation to contact the source and drain diffusion regions. An ion implantation is performed through the contact openings into the bottoms of the source and drain wells to control the device trigger voltage and position the discharge current far away from the surface, which increases the device ESD performance significantly.